Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancelled)

Claim 2 (previously presented): An encoder for motion-compensated video, comprising:

(a) first circuitry operable to extract motion data and texture data for a plurality of groups of pixels of input digital video; and

(b) second circuitry coupled to an output of said first circuitry, said second circuitry operable to aggregate said motion data and to aggregate said texture data and to insert a resynchronization word between said aggregated motion data and said aggregated texture data.

Claim 3 (previously presented): The encoder of claim 2, wherein:

(a) each of said group of pixels are the pixels of a 16 by 16 macroblock of pixels of a frame.

Claim 4 (previously presented): The encoder of claim 2, wherein:

(a) each of said group of pixels are the pixels of a 16 by 16 macroblock of pixels of a frame and lying within an object within said frame.

Claim 5 (previously presented): The encoder of claim 2, wherein:

(a) each of said group of pixels are the pixels of an 8 by 8 block of pixels of a frame.

Claim 6 (previously presented): The encoder of claim 2, wherein:

(a) each of said group of pixels are the pixels of an 8 by 8 block of pixels of a frame and lying within an object within said frame.

Claim 7 (previously presented): The encoder of claim 2, further comprising:

(a) third circuitry coupled to said second circuitry and operable to encode said motion data with a variable length code.

Claim 8 (previously presented): The encoder of claim 2, further comprising:

(a) third circuitry coupled to said second circuitry and operable to encode said texture data with a variable length code.

Claim 9 (previously presented): The encoder of claim 2, wherein:

(a) said first circuitry is also operable to extract shape data for an image object which includes said groups of pixels; and

(b) said second circuitry is also operable to insert a second resynchronization word which separates said shape data from said aggregated motion data and said aggregated texture data.

Claim 10 (currently amended): The encoder of claim 2, wherein:

(a) said first circuitry is a programmable processor executing a first program which is stored in a memory coupled to said programmable processor; and

(b) said second circuitry is said programmable processor executing a second program which is stored in said memory.

Claim 11 (previously presented): A decoder for motion-compensated video, comprising:

(a) first circuitry operable to interpret a first sequence of symbols as aggregated motion data of groups of pixels and interpret a second sequence of symbols as aggregated texture data of said groups of pixels wherein said first sequence and said second sequence are separated by a resynchronization word.

Claim 12 (previously presented): The decoder of claim 11, wherein:

(a) each of said group of pixels are the pixels of a 16 by 16 macroblock of pixels of a frame.

Claim 13 (previously presented): The decoder of claim 11, wherein:

(a) each of said group of pixels are the pixels of a 16 by 16 macroblock of pixels of a frame and lying within an object within said frame.

Claim 14 (previously presented): The decoder of claim 11, wherein:

(a) each of said group of pixels are the pixels of an 8 by 8 block of pixels of a frame.

Claim 15 (previously presented): The decoder of claim 11, wherein:

(a) each of said group of pixels are the pixels of an 8 by 8 block of pixels of a frame and lying within an object within said frame.

Claim 16 (previously presented): The decoder of claim 11, further comprising:

(a) a variable-length-code decoder coupled to an input of said first circuitry and operable to output said motion data.

Claim 17 (previously presented): The decoder of claim 11, further comprising:

(a) a variable-length-code decoder coupled to an input of said first circuitry and operable to output said texture data.

Claim 18 (previously presented): The decoder of claim 11, wherein:

(a) said first circuitry is also operable to interpret a third sequence of symbols as shape data for an image object which includes said groups of pixels, wherein a second resynchronization word separates said shape data from said aggregated motion data and said aggregated texture data.

Claim 19 (currently amended): The decoder of claim 11, wherein:

(a) said first circuitry is a programmable processor executing a first program which is stored in a memory coupled to said programmable processor.